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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent of:

Narihiro MOROSAWA

Patent No.: 6,818,495 B2

Issue Date: November 16, 2004

Title: THIN FILM TRANSISTOR, THIN FILM TRANSISTOR
ARRAY SUBSTRATE, LIQUID CRYSTAL DISPLAY DEVICE,
AND ELECTROLUMINESCENT DISPLAY DEVICE

REQUEST FOR CERTIFICATE OF CORRECTION
OF USPTO ERRORS UNDER RULE 322

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Certificate
FEB 24 2005
of Correction

Sir:

It is respectfully requested that a Certificate of Correction be issued in order to correct the errors made by the USPTO, as specified in the attached copy of the Certificate of Correction form (PTO-1050) which has been completed according to the Notice in 862 O.G. 2.

Respectfully submitted,

PARKHURST & WENDEL, L.L.P.

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February 11, 2005

Date
RWP/mhs

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FEB 28 2005

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UNITED STATES PATENT AND TRADEMARK OFFICE CERTIFICATE OF CORRECTION

PATENT NO : 6,818,495 B2
DATED : November 16, 2004
INVENTOR(S) : Narihiro MOROSAWA

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Claim 1, line 33 (Column 22, about printed line 57),
change "piorcing" to --piercing--; and "end" to --and--.

Claim 3, line 3 (Column 23, about printed line 3), change
"stop" to --step--.

Claim 3, line 6 (Column 23, about printed line 6), change
"law" to --low--.

Claim 4, line 3 (Column 23, about printed line 14),
change "C." to --C--.

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~~concentration-doped drain region and a high concentration-doped drain~~
 region, the low concentration-doped drain region being in contact with the
 channel region, the high concentration-doped drain region having a dopant
 concentration higher than that of the low concentration-doped drain region
 5 and being connected to the channel region via the low concentration-doped
 drain region; and

the drain electrode is in contact with the high concentration-doped
 drain region.

13. A thin film transistor according to claim 11, wherein the channel
 10 region consists of only the high melting point region, the high melting point
 region being composed of polycrystalline silicon, the source region consists
 of only the first low melting point region, the first low melting point region
 being composed of polycrystalline germanium, and the drain region
 consists of only the second low melting point region, the second low melting
 15 point region being composed of polycrystalline germanium.

14. A thin film transistor according to claim 11, wherein the channel
 region consists of only the high melting point region, the source region has
 a polycrystalline silicon layer and a polycrystalline germanium layer, the
 polycrystalline germanium layer being the first low melting point region,
 20 and the drain region has a polycrystalline silicon layer and a
 polycrystalline germanium layer, the polycrystalline germanium layer
 being the second low melting point region.

allowed
 claim 1

15. A method of producing a thin film transistor comprising:

forming a semiconductor thin film on an insulating substrate, the semiconductor thin film composed of a first semiconductor;

patterning the semiconductor thin film by photolithography and etching to form a patterned semiconductor thin film;

5 forming a first electrically insulating film so as to cover the patterned semiconductor thin film;

subsequent to the step of forming a first electrically insulating film, forming a gate electrode on the patterned semiconductor thin film;

implanting ions having group IVB atoms into a portion of the
10 patterned semiconductor thin film to form a pair of low melting point regions on the patterned semiconductor thin film, the low melting point regions being spaced apart from each other and composed of a second semiconductor;

doping the regions where the pair of the low melting point regions
15 have been formed with a dopant to form a source region, a drain region, and a channel region, such that the source and drain regions are doped with the dopant and that the channel region is not doped with the dopant and is sandwiched between the source region and the drain region;

forming a second electrically insulating film so as to cover the gate
20 electrode;

forming a source electrode and a drain electrode, the source electrode piercing through the first and second electrically insulating films on the source region and being electrically insulated from the gate electrode, the drain electrode piercing through the first and second electrically insulating
25 films on the drain region and being electrically insulated from the gate

electrode and electrically connected to the drain electrode; and

heating the source region and the drain region at a predetermined temperature to activate the dopant contained in the source region and the drain region.

- 5 16. A method of producing a thin film transistor according to claim 15, further comprising a step of crystallizing a predetermined region in the semiconductor thin film by heating the predetermined region.

*allowed
claim 3*

- 10 17. A method of producing a thin film transistor according to claim 16, wherein the method further comprises, subsequent to the (step) of doping, additionally doping a portion of the drain region with the dopant to form a low concentration-doped drain region and a high concentration-doped drain region, the (low) concentration-doped drain region having not been subjected to the additional doping and in contact with the channel region, the high concentration-doped drain region having been subjected to the additional
15 doping and having a dopant concentration higher than the low concentration-doped drain region.

*allowed
claim 4*

18. A method of producing a thin film transistor according to claim 16, wherein in the step of heating, the predetermined temperature is (600°C) or lower.
- 20 19. A method of producing a thin film transistor according to claim 16, wherein:

in the step of forming a semiconductor thin film, the semiconductor thin film is an amorphous silicon thin film;

in the step of implanting ions, the group IVB atoms are germanium atoms; and

in the step of crystallizing, the channel region, the source region, and the drain region are subjected to the crystallizing.

5 20. ~~A method of producing a thin film transistor, comprising:~~

forming a first thin film composed of a third semiconductor on an insulating substrate;

patterning the first thin film by photolithography and etching to form a source thin film and a drain thin film;

10 doping the first thin film or the source and drain thin films with a dopant to form a source region in the source thin film and a drain region in the drain thin film, such that the source and drain regions are doped with the dopant;

subsequent to the step of patterning a first thin film, forming a second
15 thin film over the insulating substrate, the second thin film composed of a fourth semiconductor having a melting point higher than that of the third semiconductor;

patterning the second thin film by photolithography and etching to form a channel thin film connecting the source thin film and the drain thin
20 film;

forming a first electrically insulating film so as to cover the source thin film, the drain thin film, and the channel thin film;

subsequent to the step of forming a first electrically insulating film,
~~forming a gate electrode above the channel thin film;~~